Common-Mode EMI Noise Modeling and Reduction With Balance Technique for Three-Level Neutral Point Clamped Topology

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Abstract—**This paper develops a common-mode (CM) electromagnetic interference noise model for a three-level neutral point clamped topology. Compared with existing modeling techniques with only one CM noise source, two extra important CM noise sources and their characteristics are identified and derived for an accurate CM noise model. The impedances of CM noise path are also extracted. Based on the developed CM noise model, the CM noise spectrum can be well predicted. The effect of CM noise paths on CM noise is discussed based on two different LCL filters. A CM noise reduction technique with a balance bridge at a large impedance ratio is proposed based on the developed model. The technique can be easily implemented at low cost. Both simulations and experiments validate the developed theory and technique.**

Index Terms—**Balance technique, common mode (CM), electromagnetic interference (EMI), EMI modeling, EMI reduction, neutral point clamped topology.**

I. INTRODUCTION

THE three-level neutral point clamped (3L-NPC) topology is one of the most popular multilevel topologies used in the industry [1]. It provides a simple solution to extend voltage and power ranges of the existing two-level voltage source inverter (2L-VSI) since the commutation voltages of all semiconductor devices are half of the dc-link voltage [2].

One important application for 3L-NPC topology is to work as a bidirectional interface between the utility grid and various dc sources such as renewable energy and energy storage. When the pulse width modulation technique is employed, the high-voltage slew rates (*dv/dt*) caused by switching operations are major conductive common mode (CM) and radiated electromagnetic interference (EMI) noise sources. Standards such as EN 55022, EN 61000-6-3, and EN 61000-6-4 specify the limits of EMI emissions from power electronics devices for residential, commercial, and industrial applications.

In order to investigate the EMI characteristics of power electronics systems, EMI models must be first developed. EMI reduction techniques can be developed based on these developed models. The models can also be used to predict EMI, evaluate the effectiveness of EMI filters and EMI reduction techniques. Although a lot of EMI modeling work has been conducted for 2L-VSIs [3]–[11], very little serious work has been done on 3L-NPC topology. A 2L-VSI has two switches per phase leg and a 3L-NPC inverter has four switches and two diodes. As a result, the number of high *dv/dt* nodes increases from one to three per phase when a 3L-NPC instead of 2L-VSI is used. The influence of the two added high *dv/dt* nodes are missed in the analysis of existing works [12], [13]. It greatly complicates the EMI analysis.

The complexity can be illustrated in Fig. 1. In Fig. 1, a three-phase grid-connected 3L-NPC inverter with an LCL harmonic filter has three nodes with different *dv/dt* in each phase. The dc bus also has a different *dv/dt* against ground. For example, in phase A, if dc component is not considered, there are four different *dv/dts* against the ground potential at nodes *A*, *A1*, *A2* and the dc bus and all of them can contribute to CM EMI noise. The parasitic capacitances between these nodes and ground are determined by the packaging of the semiconductor devices and the physical structure and connections of device heatsinks and dc bus. So they are different too. Because of this, it is inappropriate to simply characterize 3L-NPC topology using a single CM noise source as did in existing literatures [4], [6]–[14]. A more comprehensive and accurate model needs to be developed for 3L-NPC topology.

In this paper, the CM EMI noise model is first developed for the three-phase 3L-NPC topology. Based on the developed model, CM noise is predicted and compared with the measurement results. A CM noise reduction technique with a bridge at a large impedance ratio is proposed based on the developed model. Finally, both simulation and experimental results verified the proposed noise reduction technique.

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II. CM EMI MODEL FOR NPC INVERTERS

Two basic approaches have been used to characterize EMI emissions: time-domain and frequency domain EMI modeling
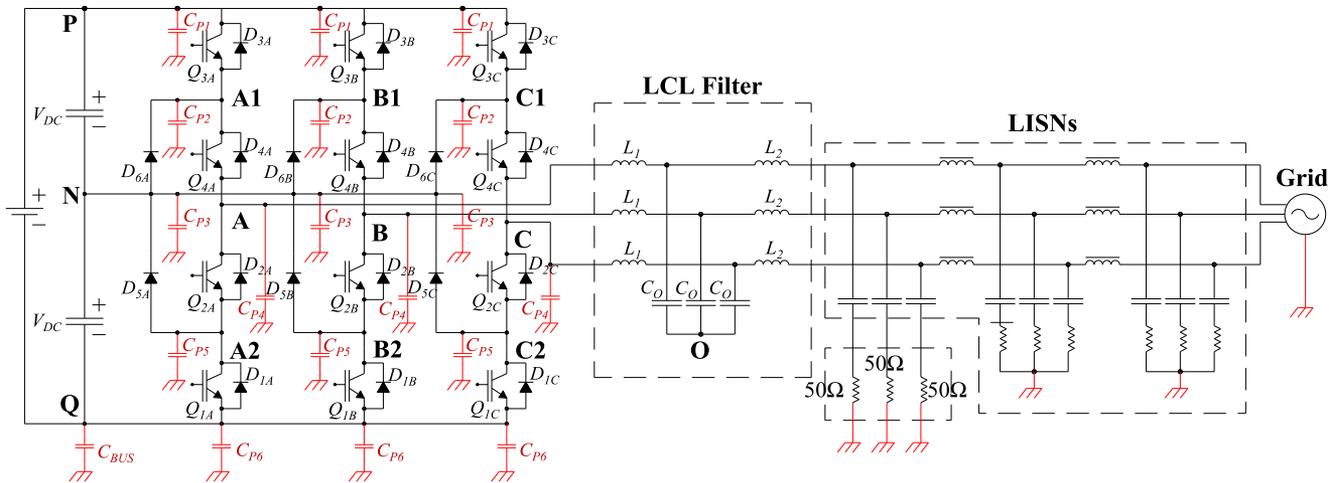
Fig. 1.   Topology of a three-phase grid-connected 3L-NPC converter with LCL filters.

[5], [7]. Both approaches involve the modeling of EMI noise sources and noise propagation paths. The difference between the two mainly lies in the noise source modeling.

For the time-domain approach, researchers characterize the noise source with physical structure-based [3] or behavior-based device model [9]. The model is either developed from parameter extraction or the turn-on and turn-off dynamics of the semiconductor devices. The models are then simulated with software such as Saber or Pspice to obtain the current waveforms that flowing through the line impedance stabilization networks (LISNs). A discrete Fourier transformation (DFT) is used in postprocessing to predict the noise spectrum. The upper limit of the frequency of DFT is the key for setting the simulation time step. For conducted EMI noise, standards such as EN 61000-6-3 define the frequency range from 150 kHz to 30 MHz. The maximum allowable time step is about 16 ns according to the Nyquist–Shannon sampling theorem. Because of this, for a complicated circuit with multiple parasitic components, simulation could be very time consuming [7] and convergence problems may occur [6].

Frequency domain analysis is another approach used for EMI analysis. Substitution theory is applied in this approach to replace the original switches with noise sources in order to linearize the circuit [15]. The rest of the circuit will not be influenced if the noise sources have the same time-domain waveforms as the originals. One method to get the time-domain waveforms is through measurement. If the switching waveforms are properly sampled, the waveforms can be rebuilt with the sampled data and transformed to frequency domain using DFT algorithms. Some papers simplify the process by assuming the switching waveforms are purely trapezoidal [4], [6], [8], [10]. Based on the Laplace transformation, the analytical expressions can be derived. However, actual switching waveforms have high-frequency (HF) ringing waveforms, so the predicted noise spectrum may not be accurate at HFs.

One issue which must be solved of using the frequency-domain approach is that because only one noise source should be used at a time, the noise sources of all phases must be combined

to a single CM noise source before this CM noise source can be replaced with its noise spectrum for EMI prediction. This is due to the fact that if the noise sources are replaced with their spectra before they are combined to one source, the phase information will be lost. Therefore, when the phase information cannot be preserved, it is better to keep the analysis in time domain. This does not mean physical structure-based device models must be used for time-domain analysis. The equivalent circuit developed for frequency-domain analysis can still be used, but the noise sources must be replaced by their time-domain waveforms other than their spectra. This approach will be used in this paper.

A. Noise Source Modeling

The noise source modeling for the 3L-NPC topology starts from a single-phase analysis. Fig. 2(a) shows its phase A leg connecting to the dc bus. Q_{1A}–Q_{4A} are IGBTs or other semiconductor devices and D_{1A}–D_{6A} are diodes.

The first step is to extract major CM parasitic capacitances of noise sources. C_{P1}–C_{P6} are the major CM parasitic capacitances. If the phase leg is built by discrete semiconductor devices, C_{P6} could be ignored due to the small emitter and anode to ground/heatsink CM parasitic capacitance of Q_{1A} and D_{1A}. C_{P1}, C_{P4} and C_{P5} are the collector and cathode to ground/heatsink CM parasitic capacitances of Q_{3A} & D_{3A}, Q_{2A} & D_{2A}, Q_{1A} & D_{1A}. C_{P3} is the cathode to ground/heatsink CM parasitic capacitance of D_{5A}. C_{P2} is the combined CM parasitic capacitances between emitter and anode of Q_{4A}, D_{4A} and D_{6A} and ground/heatsink. Because of this, C_{P2} could be bigger than C_{P5}. This indicates that CM parasitic capacitance of the upper and lower parts of the phase leg is asymmetric when discrete devices are used.

If the whole phase leg is integrated into one power module, such as the SEMIKRON SKiiP 28MLI07E3V1 used in the prototype of this paper, the values of C_{P1}–C_{P6} are determined by its packaging. Fig. 3 shows the internal packaging of an integrated 3L-NPC phase leg with IGBTs and diodes integrated. The CM parasitic capacitance of each semiconductor device
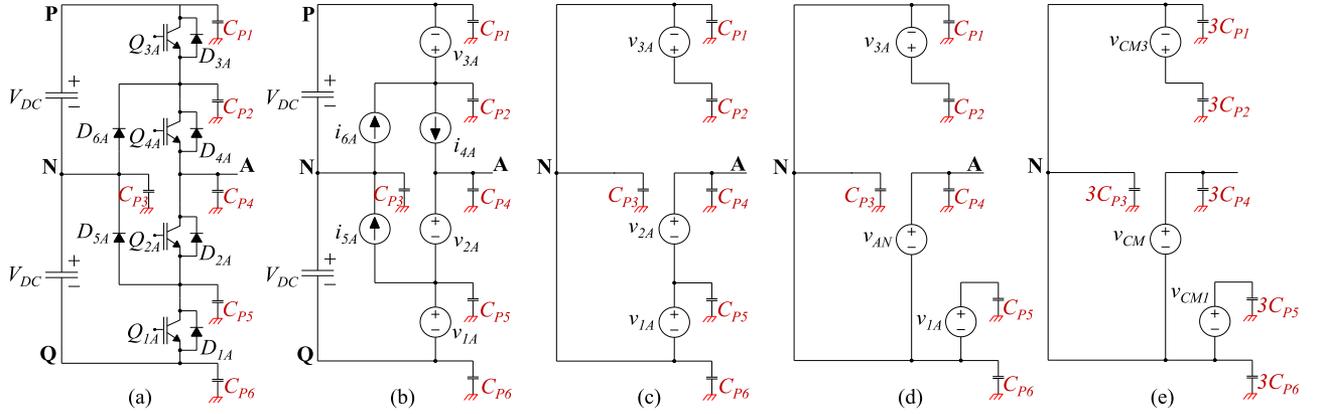
Fig. 2. EMI modeling the 3L-NPC topology: (a) phase A leg connecting to the dc bus; (b) replace the semiconductor switches with noise sources; (c) remove the noise sources that generates no CM noise; (d) combine noise sources v_{1A} and v_{2A} into v_{AN}; and (e) three-phase CM EMI noise model for the 3L-NPC inverter.
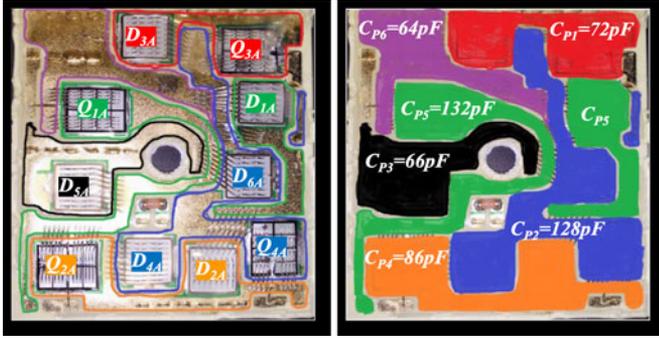

Fig. 3. Parasitic capacitances of SEMIKRON SKiiP 28MLI07E3V1.

is determined by the area of conductor layer of each device shown in Fig. 3. The capacitances were measured with a Keysight 4294A precision impedance analyzer after the module is installed on the heatsink. The measured capacitances are shown in Fig. 3. It shows that C_{P2} (128 pF) and C_{P5} (132 pF) are very close in this case.

The next step is to apply the substitution theory to the semiconductor switches of the circuit [15], [16]. As shown in Fig. 2(b), the three branches composed of Q_{1A} & D_{1A}, Q_{2A} & D_{2A}, Q_{3A} & D_{3A} are replaced by three noise voltage sources v_{1A}, v_{2A}, and v_{3A}. The branch composed of Q_{4A} & D_{4A} is replaced by a noise current source i_{4A}. D_{5A} and D_{6A} are replaced by two noise current sources i_{5A} and i_{6A}. All noise sources shall have the same time-domain waveforms as the original branches they replaced with, and it is important to note that voltage sources cannot be in parallel and current sources cannot be in series.

The circuit can be further simplified based on superposition theory. In the analysis, the dc capacitors are treated as short circuits to CM noise due to their small ac impedances. The current sources i_{4A}, i_{5A}, and i_{6A} can be eliminated in the final CM EMI model since they are shorted by noise sources v_{1A}, v_{2A}, v_{3A} and the dc capacitors. The noise model becomes Fig. 2(c).

In Fig. 2(c), v_{1A} and v_{2A} are further transformed into v_{1A} and v_{AN} in Fig. 2(d).

In Figs. 1 and 2, if v_{CM}, v_{CM1}, v_{CM2}, and v_{CM3} are defined as

$$v_{\mathrm{CM}} = \frac{v_{\mathrm{AN}} + v_{\mathrm{BN}} + v_{\mathrm{CN}}}{3} \tag{1}$$

$$v_{\mathrm{CM1}} = \frac{v_{1A} + v_{1B} + v_{1C}}{3} \tag{2}$$

$$v_{\mathrm{CM2}} = \frac{v_{2A} + v_{2B} + v_{2C}}{3} \tag{3}$$

$$v_{\mathrm{CM3}} = \frac{v_{3A} + v_{3B} + v_{3C}}{3}. \tag{4}$$

It is obvious that

$$v_{\mathrm{CM1}} + v_{\mathrm{CM2}} = v_{\mathrm{CM}}. \tag{5}$$

The three-phase CM EMI noise model for the 3L-NPC inverter is therefore shown in Fig. 2(e). All CM parasitic capacitances are tripled in the three-phase model because the CM parasitic capacitances of three phases are in parallel.

It is assumed that two series IGBTs have the same voltage drops at off states, the relationships between switching states and the corresponding noise sources can be derived in Table I.

From Table I

$$v_{2A} - v_{3A} = v_{2B} - v_{3B} = v_{2C} - v_{3C} = V_{\mathrm{DC}}. \tag{6}$$

By substituting (6) into (3) and (4), the relationship between two CM noise sources is

$$v_{\mathrm{CM2}} - v_{\mathrm{CM3}} = V_{\mathrm{DC}}. \tag{7}$$

By substituting (7) into (5), it is found as

$$v_{\mathrm{CM1}} + v_{\mathrm{CM3}} = v_{\mathrm{CM}} - V_{\mathrm{DC}}. \tag{8}$$

This means that only two of the three CM noise sources in Fig. 2(e) are independent.

B. Noise Propagation Path Modeling

The impedance of the EMI propagation path is measured using a Keysight 4294A precision impedance analyzer from

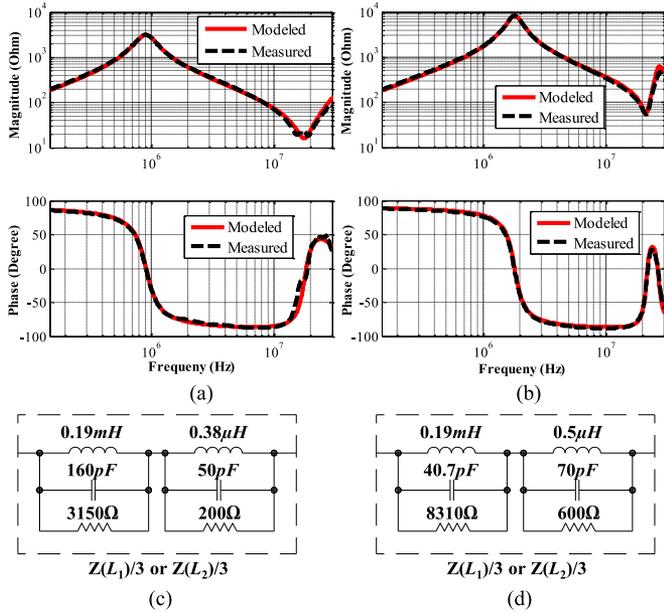| $v_{A/B/CN}$	$Q_{1A/B/C}$	$Q_{2A/B/C}$	$Q_{3A/B/C}$	$Q_{4A/B/C}$	$v_{1A/B/C}$	$v_{2A/B/C}$	$v_{3A/B/C}$
$+V_{DC}$	OFF	OFF	ON	ON	V_{DC}	V_{DC}	0
0	OFF	ON	OFF	ON	V_{DC}	0	$-V_{DC}$
$-V_{DC}$	ON	ON	OFF	OFF	0	0	$-V_{DC}$

Fig. 4.   Modeling of LCL filters: (a) measured and modeled impedance of three L_1s in parallel for LCL filter 1; (b) measured and modeled impedance of three L_1s in parallel for LCL filter 2; (c) two-stage inductor model for LCL filter 1; and (d) two-stage inductor model for LCL filter 2.

Fig. 5.   Final CM EMI noise system model.

150 kHz to 30 MHz. The dc bus parasitic capacitance $C_{\rm BUS}$ in Fig. 1 is measured as 0.3 nF.

For the LCL filter, in order to investigate the propagation path's influence on CM EMI noise, two different LCL filters are tested in the experiments. The capacitor C_O for both filters is 20 μF. The inductors L_1 and L_2 for both filters are 0.57 mH. However, the equivalent parallel capacitances (EPCs) of the inductors in these two filters' inductors are different. Fig. 4(a) and (b) show the CM impedance curves of three L_1s in parallel for both filters. Since L_2 has the almost same impedance curve as L_1, it is not shown here.

For filter 1, the inductors' parallel resonance caused by the EPCs and the inductance is at around 1 MHz in Fig. 4(a). For filter 2, the inductors' parallel resonance caused by the EPCs and the inductance is at around 2 MHz in Fig. 4(b). This indicates the EPCs are much smaller than those in filter 1. There are also high-order series resonances and parallel resonances above 10 MHz in both impedance curves. Since for CM currents, the inductors of three phases are in parallel, the CM inductance is 0.19 mH. The impedance in Fig. 4(a) and (b) can be approximately modeled using the two-stage inductor models with extracted parameters in Fig. 4(c) and (d), respectively. The comparisons between the
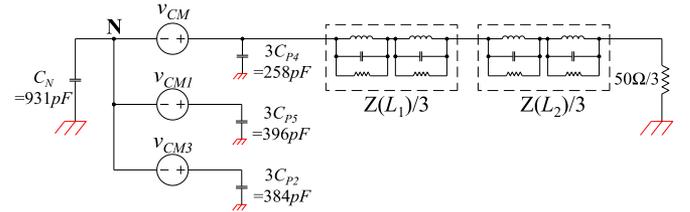
modeled and measured impedance curves are also shown in Fig. 4 (a) and (b). They match very well. In the two filters, Y connected C_os do not conduct CM currents because the star point O in Fig. 1 is floating.

The CM impedance of LISNs is simply modeled as a 50 Ω/3 resistor since each phase is 50 Ω. More accurate impedance can be found in datasheet.

C. Final CM EMI Noise Model

The final CM EMI noise system model including both the noise source model and the noise propagation path model is in Fig. 5. C_N is the sum of all the parasitic capacitances between the dc bus and the ground

$$C_N = 3C_{P1} + 3C_{P3} + 3C_{P6} + C_{\rm BUS}. \qquad (9)$$

Existing literatures on 3L topology only considered one noise source $v_{\rm CM}$ of the CM EMI model in Fig. 5. In this paper, it is proved that three noise sources are necessary to model the 3L-NPC topology. The model reveals that, the suppression of noise source $v_{\rm CM}$ only cannot fully solve the CM EMI issue in the 3L-NPC inverter. Noise generated by $v_{\rm CM1}$ and $v_{\rm CM3}$ must be considered and suppressed as well.

D. CM EMI Noise Prediction

The NPC inverter in Fig. 1 has a switching frequency of 20 kHz and the dc bus voltage is 200 V. The voltage sources in Fig. 5 are replaced with simulated time-domain voltage waveforms. The simulated CM voltage waveforms are almost the same as the measured. Fig. 6 shows the comparison between the simulated and the measured spectra at a sample rate of 50 MSa/s for the CM noise source $v_{\rm CM}$. The difference is very small. The simulated CM noise spectra flowing through 50 Ω/3 LISN resistance with LCL filters 1 and 2 are compared with the measured ones in Fig. 7 (a) and (b), respectively. The predicted noise spectra match the measured one very well.
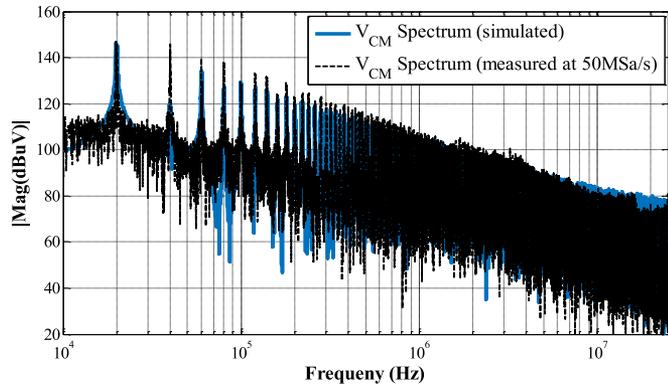
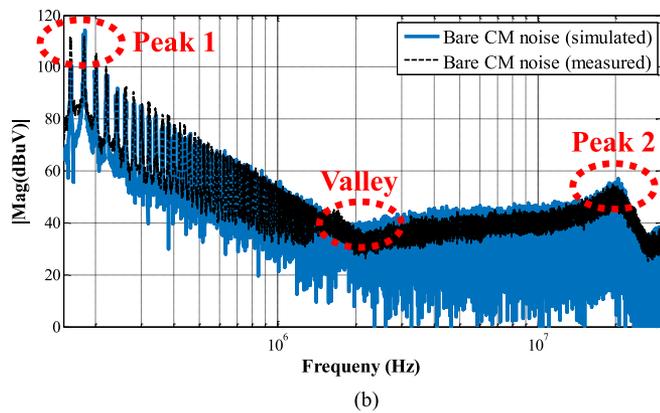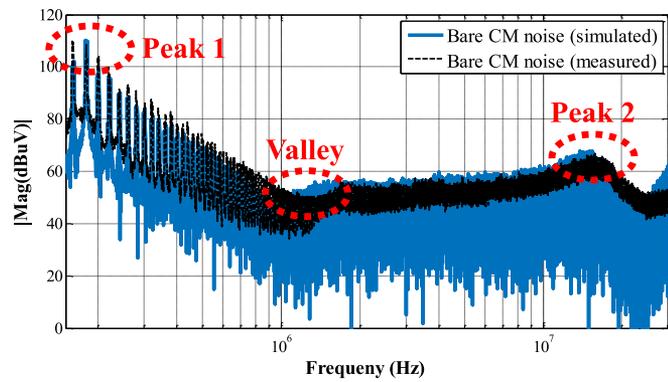Fig. 6. Comparison between the measured and simulated noise spectra of V_{CM}.

(a)

(b)

Fig. 7. CM noise comparison: (a) with LCL filter 1 and (b) with LCL filter 2.

Fig. 8. CM noise model simplification after circuit modification: (a) combining v_{CM1} and v_{CM3}; (b) simplification by adding C_{CM}; and (c) final simplified model.

in Fig. 7(b) are determined by the impedance peaks in Fig. 4(a) and (b), respectively, as discussed in [17] and [18]. For the same reason, the frequencies of peak 2 are also determined by the impedance valleys in Fig. 4(a) and (b).

III. CM NOISE CANCELLATION WITH BALANCE

A. Conditions for Model Simplification and Balance

The balance technique has been proposed and used in several papers for EMI noise reduction [15], [19], [20]. In most applications, the technique is only used to suppress one noise source at a time. Therefore, in order to apply the balance technique to the CM EMI noise model, which has three noise sources in Fig. 5, some efforts are needed.

First, C_{P2} (128 pF) and C_{P5} (132 pF) are very close so they can be treated as equal. If they are unequal, three small capacitors can be added to the smaller one to make them equal. This can be done by adding three small capacitors between the collectors of IGBTs and the heatsink of the three legs. Based on the Thevenin theorem, v_{CM1} and v_{CM3} branches can then be equivalent to a new branch in Fig. 8 (a). From (8), the new equivalent noise source $(v_{\mathrm{CM1}} + v_{\mathrm{CM3}})/2$ is equal to $v_{\mathrm{CM}}/2$ because its dc component $V_{\mathrm{DC}}/2$ does not contribute to CM noise.

Second, a Y-capacitor C_{CM} is added between dc bus point N and the ground. C_{CM} is big enough so that

$$C_{\mathrm{CM}} + C_N >> 3\left(C_{P5} + C_{P2}\right). \qquad (11)$$

Then, the CM noise current i_C in Fig. 8(a) is determined by $v_{\mathrm{CM}}/2$ and $3(C_{P5} + C_{P2})$ only. Both $v_{\mathrm{CM}}/2$ and the impedance of $3(C_{P5} + C_{P2})$ in Fig. 8(a) can be doubled without changing i_C as shown in Fig. 8(b). Fig. 8(b) can be further transformed to Fig. 8(c) based on the network theory. C_J is the equivalent to the three-phase output parasitic capacitance of the

The noise peaks and valleys of the noise spectra in Fig. 7 can be explained by the equivalent noise model in Fig. 5. The frequency f_{peak1} of the peak 1 is determined by the total CM parasitic capacitance and CM inductance in

$$f_{\mathrm{peak1}} = \\ 1 \Big/ \left[2\pi \sqrt{\left(C_N + 3C_{P2} + 3C_{P4} + 3C_{P5}\right)\left(L_1 + L_2\right)/3} \right] \qquad (10)$$

so there is no difference for the two filters. The frequencies of the noise valleys around 1 MHz in Fig. 7(a) and around 2 MHz

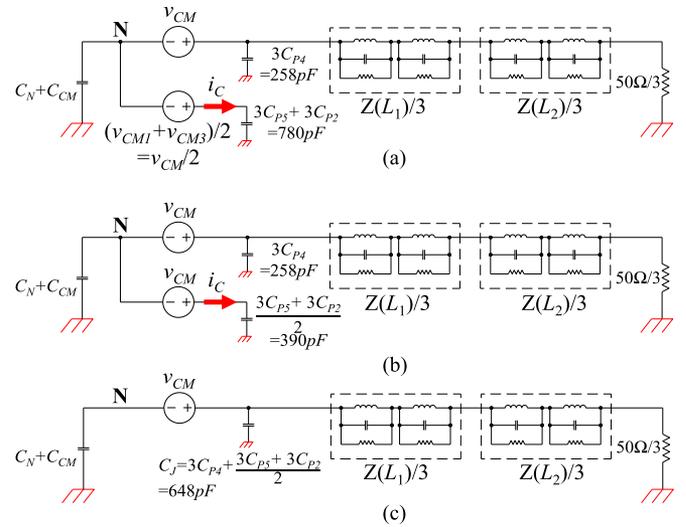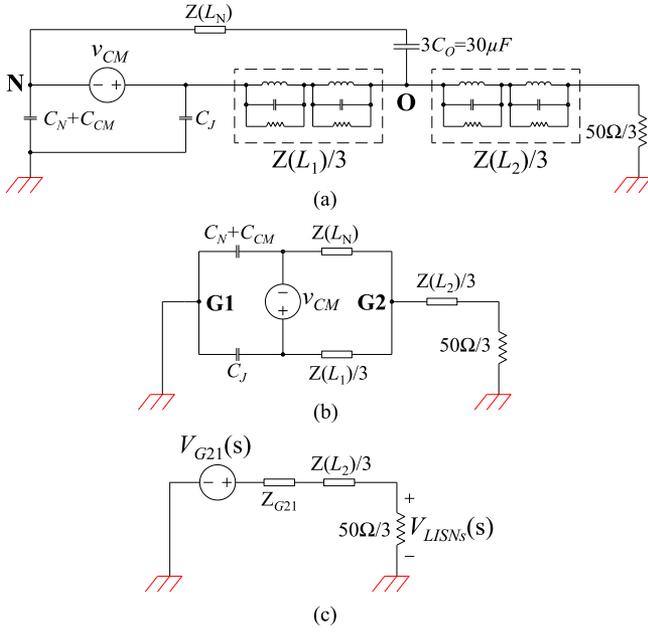Fig. 9. Equivalent circuit with balance technique: (a) L_N is added for balance; (b) Wheatstone bridge representation; and (c) using Thevenin equivalent circuit for the Wheatstone bridge.

3L-NPC inverter

$$C_J = 3C_{P4} + (3C_{P5} + 3C_{P2})/2. \qquad (12)$$

In a summary, the 3L-NPC topology can be modeled with one noise voltage source v_{CM} when the following two conditions are met: 1) C_{P2} equals to C_{P5} and 2) the total dc bus to ground capacitance is much larger than $3(C_{P5} + C_{P2})$. If these two conditions cannot be met, the generalized model in Fig. 5 should be used. The reduced CM EMI noise model in Fig. 8(c) is a special case of the generalized model.

B. Bridge With a Large Impedance Ratio for Noise Reduction

The balance technique is applied to the simplified CM noise model in Fig. 9(a). An inductor L_N is added between the neutral O on ac side and the neutral N on dc side. Equivalently, a Wheatstone bridge is developed as shown in Fig. 9(b). If the impedance of $3C_O$ is much smaller than the impedance $Z(L_N)$ of L_N, it can be ignored here. The balance condition of the Wheatstone bridge in Fig. 9(b) is

$$\frac{C_N + C_{\text{CM}}}{C_J} = \frac{Z(L_1)}{3Z(L_N)} = k \qquad (13)$$

where $Z(L_1)$ is the impedance of inductor L_1 in each phase. When the balance condition is met, the voltage difference v_{G21} between G1 and G2 in Fig. (b) is theoretically zero so no CM currents flow through LISNs.

If there is any imbalance in the Wheatstone bridge, CM noise cannot be fully cancelled and the CM noise voltage on LISNs is given by (13) based on Thevenin equivalent circuit in Fig. 9(c)

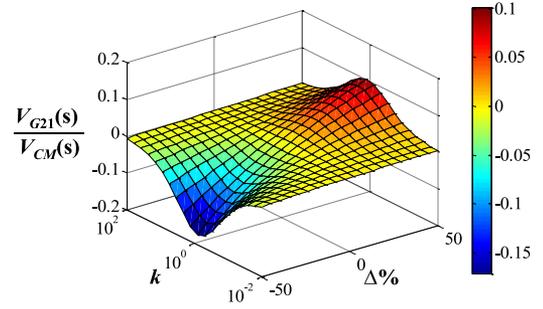$$V_{\text{LISNs}}(s) = \frac{50/3}{50/3 + Z(L_2)/3 + Z_{G21}} V_{G21}(s) \qquad (14)$$

Fig. 10. Relationship between $V_{G21}(s)$ and $V_{\text{CM}}(s)$ with respect to k and $\Delta\%$.

where $V_{G21}(s)$ and Z_{G21} are the Thevenin equivalent voltage source and impedance of the Wheatstone bridge in Fig. 9(b). There are infinite groups of C_{CM} and L_N that can be chosen to balance the Wheatstone bridge, but the good design is to select a ratio k at which the CM noise reduction is less sensitive to the undesired imbalance due to component parameters mismatch.

If $\Delta\%$ is the percentage of unbalanced impedance of $Z(L_N)$, $V_{G21}(s)$ is

$$V_{G21}(s) =$$

$$\left[\frac{Z(L_N)(1+\Delta\%)}{Z(L_1)/3 + Z(L_N)(1+\Delta\%)} - \frac{C_J}{C_J + C_N + C_{\text{CM}}} \right] V_{\text{CM}}(s). \qquad (15)$$

By substituting (13) into (15),

$$V_{G21}(s) = \left(\frac{1+\Delta\%}{k+1+\Delta\%} - \frac{1}{k+1} \right) V_{\text{CM}}(s). \qquad (16)$$

This shows how $\Delta\%$ and k influence the output of Wheatstone bridge. Fig. 10 is a 3-D graph showing $V_{G21}(s)/V_{CM}(s)$ as a function of $\Delta\%$ and k when k changes from 0.01 to 100 and $\Delta\%$ changes from -50% to 50%. It clearly shows that the highest $V_{G21}(s)$ always happen at $k = 1$. This is reasonable as it is well known that the Wheatstone bridge is most sensitive when $k = 1$. It is shown in (16) that, when k is much larger than 1 or close to 0, $V_{G21}(s)$ becomes very small and close to 0 even the bridge is significantly unbalanced. Therefore, it is better to design a k that is close to 0 or much bigger than 1 to significantly reduce CM noise. This is called noise reduction technique with a bridge at a large impedance ratio.

Since k is already bigger than 1 for the current design given that C_N is larger than C_J, (931 pF versus 648 pF), it is therefore reasonable to design a k much larger than 1. This conclusion will be further verified from Z_{G21}

$$Z_{G21} = \frac{1}{k+1} \frac{1}{sC_J} + \frac{1+\Delta\%}{k+1+\Delta\%} \frac{Z(L_1)}{3}. \qquad (17)$$

Substituting (16) and (17) into (14), yields (18) shown at the bottom of the next page. When k is much bigger than 1, (18), shown at the bottom of the next page, can be simplified as

$$V_{\text{LISNs}}(s) = \frac{50 \cdot \Delta\% \cdot V_{\text{CM}}(s)}{k[50 + Z(L_2)] + \frac{3}{sC_J} + (1+\Delta\%)Z(L_1)}. \qquad (19)$$

It shows that $V_{\mathrm{LISNs}}(s)$ is monotonic to k. When k increases, CM EMI noise flowing through LISNs will decrease. In this design, $Z(L_2)$ is equal to $Z(L_1)$. It is obvious that the bigger k is, the smaller the $V_{\mathrm{LISNs}}(s)$ is. A big C_{CM} and a small L_N should be designed to achieve high k.

However, C_{CM} cannot be too big because of line frequency grounding current limit defined in standard such as VDE 0126-1-1 as well as possible false grounding current protection trigger. At the same time, L_N should include the parasitic inductance from N to O if it is significant. The question is how to meet the balance condition (13) in a wide frequency range since $Z(L_1)$ and $Z(L_N)$ are not always inductance due to their parasitic parameters as shown by Fig. 4.

C. Coupling L_{N} with L_1 to Improve Performance

In order to minimize the influence of the parasitic parameters of L_1 and L_N on the balance, L_N should be coupled with L_1 as proposed in single-phase power electronics in [15]. In Fig. 11, L_1 and L_N are coupled in each phase. Fig. 12(a) shows an implementation of the coupled inductor, where L_N has only one turn. I_{i1}, I_{i2}, and I_{i3} are the currents flowing through the branchs 1, 2, and 3 on phase i as shown in Fig. 12(b), where $i = a$, b, c. V_{i1}, V_{i2} and V_{i3} are the voltage drops on the inductor L_1 and L_N of phase i.

In Fig. 12(b), if L_1 has n_1 turns, L_N has n_2 turns, M is mutual inductance, and L_1 and L_N are fully coupled

$$L_N = n_2^2 L_1 / n_1^2 \tag{20}$$

$$M = n_2 L_1 / n_1. \tag{21}$$

The coupled inductors are modeled with transformer models with parasitic parameters in Fig. 12 (c). R_P and C_P are the parasitic parameters of the coupled inductor reflected to the primary side of the transformer.

If the voltage drop over C_O is ignored, based on Fig. 12(c)

$$V_{i1} = sL_1 \left[I_{i1} + \frac{n_2}{n_1}(I_{a2} + I_{b2} + I_{c2}) - \frac{V_{i1}}{Z_P} \right] \tag{22}$$

$$\frac{V_{i1}}{V_{i2}} = \frac{n_1}{n_2} \tag{23}$$

where Z_P is the impedance of R_P and C_P in parallel.

If I_{01}, I_{02}, I_{03}, V_{01} and V_{02} are defined as

$$I_{01} = I_{a1} + I_{b1} + I_{c1} \tag{24}$$

$$I_{02} = I_{a2} + I_{b2} + I_{c2} \tag{25}$$

$$I_{03} = I_{a3} + I_{b3} + I_{c3} \tag{26}$$

$$V_{01} = (V_{a1} + V_{b1} + V_{c1})/3 \tag{27}$$

$$V_{02} = V_{a2} + V_{b2} + V_{c2}. \tag{28}$$

Substituting (22) to (26) into (27) and (28) yields

$$V_{01} = \frac{sL_1/3 + sL_1 n_2/n_1}{1 + sL_1/Z_P} I_{01} - \frac{sL_1 n_2/n_1}{1 + sL_1/Z_P} I_{03} \tag{29}$$

$$V_{02} = \frac{(1 + 3n_2/n_1)sL_1 n_2/n_1}{1 + sL_1/Z_P} I_{02} + \frac{sL_1 n_2/n_1}{1 + sL_1/Z_P} I_{03}. \tag{30}$$

Based on (29) and (30), the resulting decoupled circuit is shown in Fig. 12(d). And the balance condition (13) becomes

$$\frac{C_N + C_{\mathrm{CM}}}{C_J} = \frac{n_1}{3n_2} = k. \tag{31}$$

D. Discussion on the Power Loss and Size Reduction due to the Balance Technique

The implementation of the balance technique to the 3L-NPC topology needs a balance inductor L_N and a Y capacitor C_{CM}. When balance condition (31) is met, the CM currents flowing through L_N and C_{CM} can be approximately evaluated by using the Wheatstone bridge given in Fig. 9(b) with the circuit disconnected from the ground at G1 and G2. Both CM currents are small due to the large impedances of C_J and L_1. Therefore, the copper loss of the two added components is very small.

For the core loss in magnetic components, the coupling of L_N and L_1 may change the magnetic flux within the magnetic core thus influences the ac loss. However, since a large k in (31) is required for better performance of the balance technique, the number of turns n_2 for L_N is very small. Besides, as aforesaid discussed, the CM current flowing through L_N is very small so the magnetic flux change is very small too. Because of this, the core loss increase is very small. Meanwhile, the DM current flowing through L_1 is usually much larger than the CM current. Therefore, coupling of L_N with L_1 usually does not require a redesign of the existing L_1s. As shown by the example in Fig. 12(a), the one-turn L_Ns use thin copper wires, thus very little cost is introduced.

The implementation of the developed balance technique can also reduce the size of CM filters. If the CM noise is not reduced with the developed balance technique, a large CM EMI filter which is much bigger than the balance inductor L_Ns and capacitor C_{CM} must be used. This is because the CM EMI filter must have big inductance and capacitance to achieve high attenuations at low frequencies so as to meet EMI standards, and at the same time, it must conduct CM current and full DM current. It is therefore concluded that the implementation of the proposed noise reduction technique can also reduce the size of EMI filters.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

In both simulation and experiment, the number of turns n_1 for L_1 is 47. In order to have a large k, n_2 for L_N is designed as 1 and L_N is coupled with L_1. k equals to 47/3 and C_{CM} is calculated as 9.2 nF from (31).

$$V_{\mathrm{LISNs}}(s) = \frac{50k \cdot \Delta\%}{[50 + Z(L_2)](k+1+\Delta\%)(k+1) + 3(k+1+\Delta\%)/(sC_J) + (1+\Delta\%)(k+1)Z(L_1)} V_{\mathrm{CM}}(s) \tag{18}$$
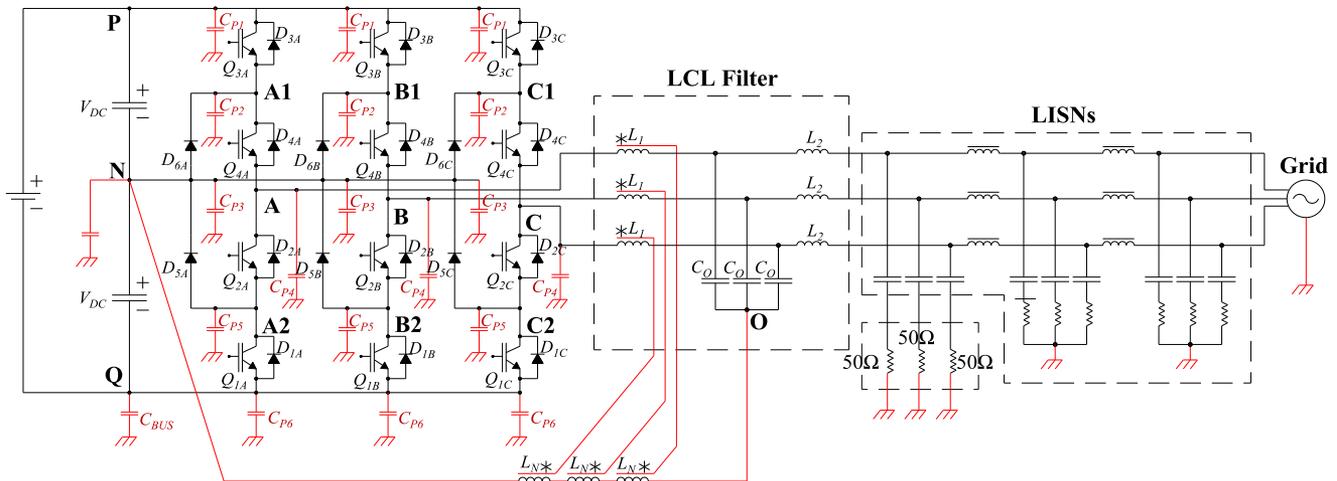
Fig. 11.   Circuit implementation of the balance technique for the three-phase topology.
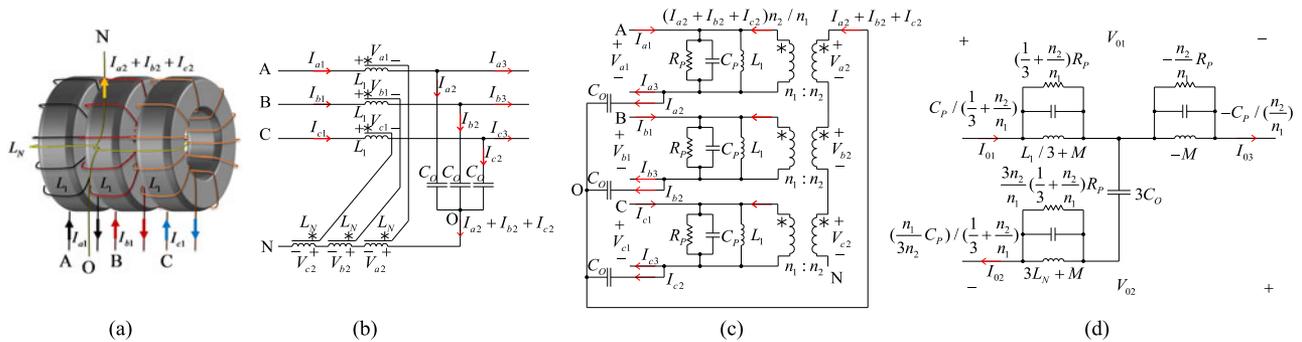

Fig. 12.   Decoupling of the three-phase coupled inductor: (a) coupled inductor; (b) coupled circuit; (c) equivalent model; and (d) decoupled circuit.
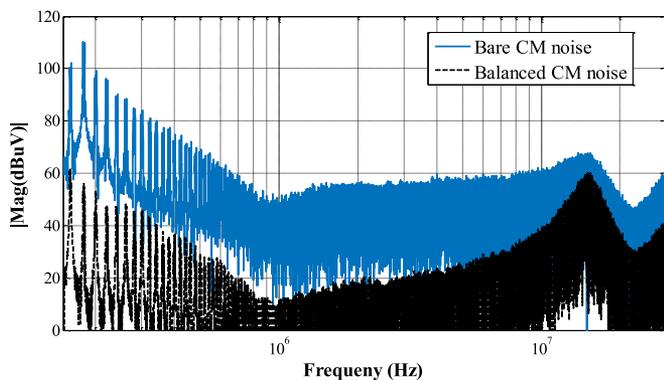

Fig. 13.   Comparison of the simulated CM EMI noise spectra before and after the implementation of balance technique (LCL filter 1).
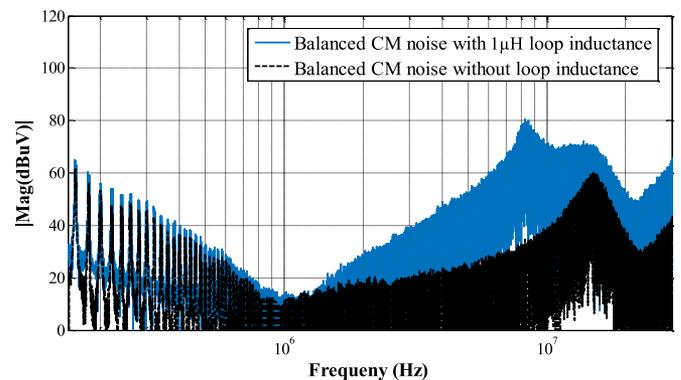

Fig. 14.   Comparison of the simulated CM EMI noise spectra under balance conditions with and without considering the parasitic inductance (LCL filter 1).

A. Simulation Verification of the Balance Technique

The simulation is conducted using Fig. 5 with all noise sources replaced with their measured time-domain waveforms. The noise is obtained from the voltage drop on LISN 50 $\Omega/3$ resistance. Fig. 13 shows the simulated CM EMI noise spectra before and after the balance technique is applied when an LCL filter 1 is used. It shows that a maximum 55-dB noise reduction is achieved and the whole noise spectrum is greatly

reduced within the concerned frequency range. This simulation does not include the parasitic inductance of the connection between O and N. The noise spectrum with balance applied and a 1-μH parasitic inductance in series with L_N is compared with that with balance applied but without parasitic inductance in Fig. 14. A detail analysis shows that the noise peak at around 8-MHz is caused by the resonance of the parasitic inductance and the paralleled EPCs of L_1 and L_2. This peak can be reduced or
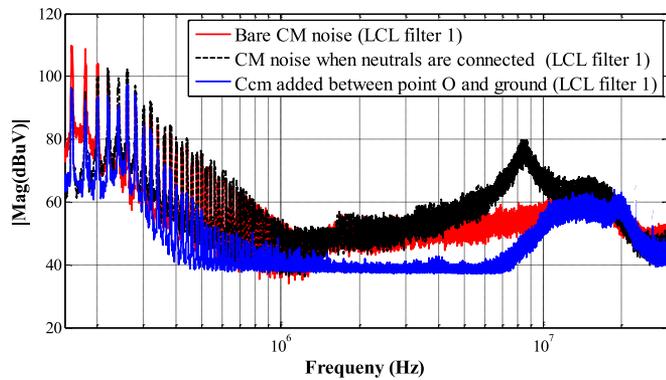
Fig. 15. Comparison of the measured CM EMI noise spectra under several conditions without the balance technique (LCL filter 1).

Fig. 16. Comparison of the measured CM EMI noise spectra with LCL filters 1 and 2 under balance conditions.

pushed to higher frequencies by reducing the EPCs or parasitic inductance. The leakage inductance of the L_N is ignored as L_N is small otherwise it should be counted as part of the parasitic inductance between N and O in the analysis of this paper.

B. Experimental Verification of the Balance Technique

A 1-kW NPC inverter prototype which has the same circuit as in Fig. 1 is used in the experiments. The dc bus voltage is 200 V. In the first experiment, the CM noise with LCL filter 1 is measured. In the second experiment, the dc neutral N and ac neutral O are connected. The CM noise is measured. In the third experiment, the two neutrals are disconnected, but the neutral O is grounded via a 9.2-nF CM capacitor. This capacitor and C_Os are now CM capacitors so they can reduce CM noise. Fig. 15 shows the results of the first three experiments. It shows that by connecting the two neutrals, low-frequency CM noise can be reduced a little bit. However, it also generates a high-frequency noise peak at around 8.3 MHz due to the parasitic inductance for the same reason as in Fig. 14. If the neutral O is grounded via a 9.2 nF, the CM noise from 500 kHz to 10 MHz can be reduced. The noise below 400 kHz and above 10 MHz is not reduced. The purpose of these experiments is to provide a fair baseline for the proposed balance technique. In all of the measured EMI spectra in this paper, the noise floor is 40 dBuV.

In the fourth experiment, the proposed large impedance ratio balance with coupled inductors ($k = 47/3$) is applied to the inverter and the CM noise is measured. The L_N has only one turn and is coupled with *L1* (47 turn). As discussed before, a 9.2-nF C_{CM} is added between the dc bus and the ground. The measured CM noise is compared with the bare CM noise with LCL filter 1 only in Fig. 16. The CM noise is greatly reduced by up to 40 dB from 150 kHz to 2 MHz. After 2 MHz, due to the resonance between the parasitic inductance and the EPCs of the L_1 an L_2, there is a noise peak at around 7.3 MHz. In the fifth experiment, the CM noise with LCL filter 2 but without balance is measured. In the sixth experiment, the CM noise with LCL filter 2 and the large impedance ratio balance with coupled inductors ($k = 47/3$) applied is measured. They are compared in Fig. 16. It shows that because the inductors of LCL filter 2 have higher impedances than the inductors of LCL filter 1 at high frequencies as shown in Fig. 4(a) and (b),
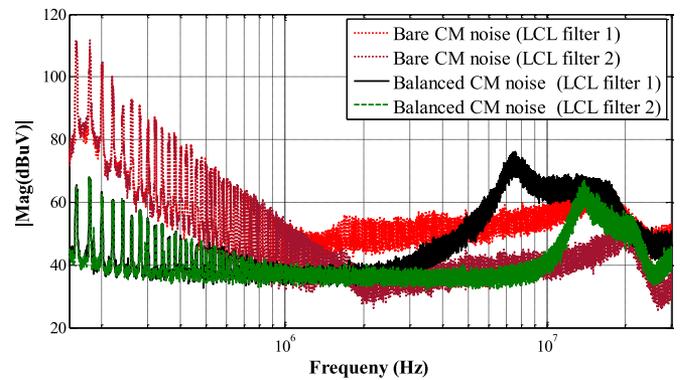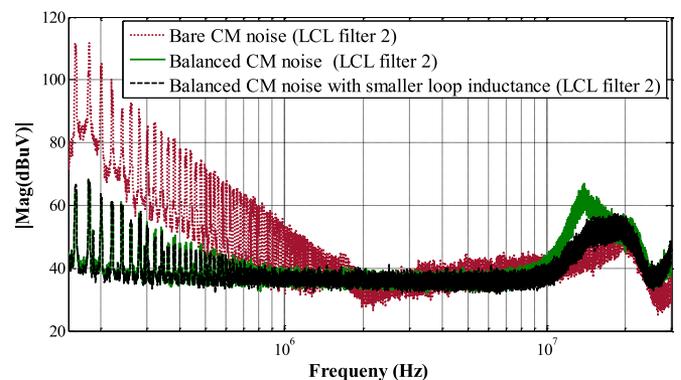

Fig. 17. Comparison of the measured CM EMI noise spectra under balance conditions with original and reduced parasitic inductances (LCL filter 2).
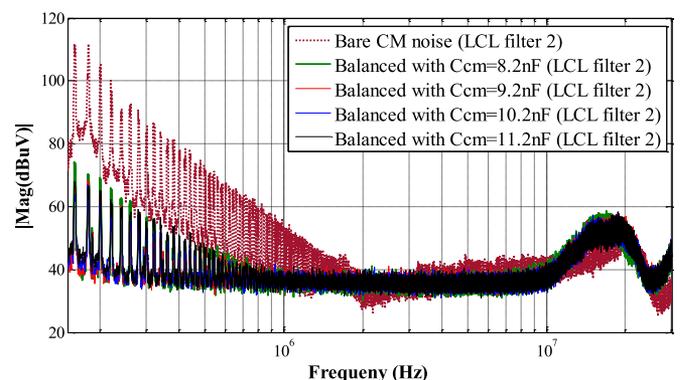

Fig. 18. Comparison of the measured CM EMI noise spectra when implementing the balance technique with different C_{CM}s (LCL filter 2).

LCL filter 2 achieves bigger noise reduction than LCL filter 1 from 2 to 30 MHz for both bare noise and balanced noise cases. Furthermore, because LCL filter 2 has much smaller EPCs than LCL filter 1, the noise peaks caused by the resonance between EPCs and parasitic inductance are increased from 7.3 to 13 MHz. Compared with the lowest CM noise in Fig. 15 with a 9.2-nF CM capacitor between O and the ground, the large impedance ratio balance technique greatly reduces both low-frequency and high-frequency noise by up to 40 dB. Fig. 17 shows that after

the parasitic inductance between O and N is reduced, the noise peak is pushed to a higher frequency.

To validate that the Wheatstone bridge at a large impedance ratio can greatly reduce CM noise even the bridge is unbalanced, different C_{CM}s are used in the balance with the LCL filter 2 in Fig. 18. It is shown that the bridge with large impedance ratios can greatly reduce CM noise even with the imbalanced C_{CM}. The noise reduction differences are within 8 dB when C_{CM} changes from 8.2 to 11.2 nF. This is very good for industrial applications.

V. Conclusion

Compared with conventional two-level topologies, the CM noise model of a three-level NPC topology has more number of noise sources and is much more complicated. In this paper, a CM noise modeling technique is developed for three-level three phase NPC topologies. Furthermore, noise source and noise propagation paths are modeled. The modeling technique is validated via both simulations and experiments. It is a powerful tool for the CM noise analysis for 3L-NPC topologies. Based on the developed model, the balance condition is also identified for CM noise reduction. A CM noise reduction technique with a bridge at a large impedance ratio is proposed for three-phase NPC topologies. It is found that the large impedance ratio and the coupling between the balance inductor and the filter inductor can greatly improve noise reduction performance in a wide frequency range even the bridge is unbalanced. The filter inductor's parasitic capacitance also plays an important role in high-frequency noise. The proposed noise reduction technique has the advantages of easy implementation, high performance and insensitive to the imbalanced impedance. Both simulations and experiments were conducted to validate the proposed large impedance ratio balance technique. It is shown that the proposed technique can greatly reduce CM noise of NPC topology in a wide frequency range.

References

[1] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multi-level voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[3] H. Zhu, J.-S. Lai, A. R. Hefner, Y. Tang, and C. Chen, "Analysis of conducted EMI emissions from PWM inverter based on empirical models and comparative experiments," in *Proc. 30th Annu. IEEE Power Electron. Spec. Conf.*, 1999, vol. 2, pp. 861–867.

[4] D. Gonzalez, J. Gago, and J. Balcells, "New simplified method for the simulation of conducted EMI generated by switched power converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1078–1084, Dec. 2003.

[5] Q. Liu *et al.*, "Experimental evaluation of IGBTs for characterizing and modeling conducted EMI emission in PWM inverters," in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, 2003, vol. 4, pp. 1951–1956.

[6] B. Revol, J. Roudet, J. L. Schanen, and P. Loizelet, "Fast EMI prediction method for three-phase inverter based on Laplace transforms," in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, 2003, vol. 3, pp. 1133–1138.

[7] J. S. Lai, X. D. Huang, E. Pepa, S. T. Chen, and T. W. Nehl, "Inverter EMI modeling and simulation methodologies," *IEEE Trans. Ind. Electron.*, vol. 53, no. 3, pp. 736–744, Jun. 2006.

[8] E. Gubia, P. Sanchis, A. Ursua, J. Lopez, and L. Marroyo, "Frequency domain model of conducted EMI in electrical drives," *IEEE Power Electron. Lett.*, vol. 3, no. 2, pp. 45–49, Jun. 2005.

[9] J. Meng and W. M. Ma, "Power converter EMI analysis including IGBT nonlinear switching transient model," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1577–1583, Oct. 2006.

[10] B. Revol, J. Roudet, J. L. Schanen, and P. Loizelet, "EMI study of three-phase inverter-fed motor drives," *IEEE Trans. Ind. Appl.*, vol. 47, no. 1, pp. 223–231, Jan./Feb. 2011.

[11] X. Gong, I. Josifovic, and J. A. Ferreira, "Modeling and reduction of conducted EMI of inverters with SiC JFETs on insulated metal substrate," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3138–3146, Jul. 2013.

[12] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 435–443, Jan. 2012.

[13] K. J. Dagan, A. Zuckerberger, and R. Rabinovici, "Fourth-arm common-mode voltage mitigation," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1401–1407, Feb. 2016.

[14] H. Zhang, S. Wang, and J. Puukko, "Common mode EMI noise modeling and prediction for a three-phase, three-level, grid tied photovoltaic inverter," in *Proc. Asia-Pacific Int. Symp. Electromagn. Compat.*, 2016, pp. 1188–1194.

[15] S. Wang and P. J. Kong, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

[16] Y. B. Chu and S. Wang, "A generalized common-mode current cancelation approach for power converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4130–4140, Jul. 2015.

[17] S. Wang, F. C. Lee, and W. G. Odendaal, "Improving the performance of boost PFC EMI filters," in *Proc. 18th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2003, vol. 1, pp. 368–374.

[18] S. Wang, F. C. Lee, and W. G. Odendaal, "Single layer iron powder core inductor model and its effect on boost PFC EMI noise," in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, 2003, vol. 2, pp. 847–852.

[19] L. Xing and J. Sun, "Conducted common-mode emi reduction by impedance balancing," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1084–1089, Mar. 2012.

[20] P. J. Kong, S. Wang, F. C. Lee, and Z. J. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.

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